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Semiconductor Manufacturing, IEEE Transactions on , Volume: 16

Issue: 2 , May 2003

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[\[Abstract\]](#) [\[PDF Full-Text \(702 KB\)\]](#) **IEEE JNL****2 Effective safety property checking using simulation-based sequential ATPG***Shuo Sheng; Takayama, K.; Hsiao, M.S.;*

Design Automation Conference, 2002. Proceedings. 39th , 10-14

June 2002

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[\[Abstract\]](#) [\[PDF Full-Text \(763 KB\)\]](#) **IEEE CNF****3 RTL level preparation of high-quality/low-energy/low-power BIST***Santos, M.B.; Teixeira, I.C.; Teixeira, J.P.; Manich, S.; Rodriguez, R.; Figueras, J.;*

Test Conference, 2002. Proceedings. International , 7-10 Oct. 2002

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**4 Cu/LKD-5109 damascene integration demonstration using FF-02 low-k spin-on hard-mask and embedded etch-stop**

*Kokubo, T.; Das, A.; Furukawa, Y.; Vos, I.; Iacopi, F.; Struyf, H.; Aelst, J.V.; Maenhoudt, M.; Tokei, Z.; Vervoort, I.; Bender, H.; Stucchi, M.; Schaekers, M.; Boullart, W.; Van Hove, M.; Vanhaelemeersch, S.; Peterson, W.; Shiota, A.; Maex, K.;*  
Interconnect Technology Conference, 2002. Proceedings of the IEEE 2002 International , 3-5 June 2002  
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[\[Abstract\]](#) [\[PDF Full-Text \(296 KB\)\]](#) [IEEE CNF](#)

---

**5 Accurate RF electrical characterisation of CSPs using MCM-D thin film technology**

*Chandrasekhar, A.; Beyne, E.; De Raedt, W.; Nauwelaers, B.;*  
Electronic Components and Technology Conference, 2002. Proceedings. 52nd , 28-31 May 2002  
Page(s): 70 -78

[\[Abstract\]](#) [\[PDF Full-Text \(1551 KB\)\]](#) [IEEE CNF](#)

---

**6 Power integrated circuit drives based on HV NMOS**

*Finco, S.; Tavares, P.; Fiore De Mattos, A.C.; Castro Simas, M.I.;*  
Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual , Volume: 4 , 23-27 June 2002  
Page(s): 1737 -1740

[\[Abstract\]](#) [\[PDF Full-Text \(534 KB\)\]](#) [IEEE CNF](#)

---

**7 On the propagation of faults and their detection in a hardware implementation of the Advanced Encryption Standard**

*Bertoni, G.; Breveglieri, L.; Koren, I.; Maistri, P.; Piuri, V.;*  
Application-Specific Systems, Architectures and Processors, 2002. Proceedings. The IEEE International Conference on , 17-19 July 2002  
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[\[Abstract\]](#) [\[PDF Full-Text \(596 KB\)\]](#) [IEEE CNF](#)

---

**8 Integrated chip-scale simulation of pattern dependencies in copper electroplating and copper chemical mechanical polishing processes**

*Tugbawa, T.E.; Park, T.H.; Boning, D.S.;*  
Interconnect Technology Conference, 2002. Proceedings of the IEEE 2002 International , 3-5 June 2002  
Page(s): 167 -169

[\[Abstract\]](#) [\[PDF Full-Text \(353 KB\)\]](#) **IEEE CNF**

---

**9 Triple implanted bipolar junction transistor**

*Fields, K.L.; Green, J.; Midkif, J.; Vu Hang;*

University/Government/Industry Microelectronics Symposium, 2001.

Proceedings of the Fourteenth Biennial , 17-20 June 2001

Page(s): 205 -208

[\[Abstract\]](#) [\[PDF Full-Text \(232 KB\)\]](#) **IEEE CNF**

---

**10 Processing design rules for reliable reflowable underfill application**

*Kallmayer, C.; Becker, K.-F.; Jung, E.; Aschenbrenner, R.; Reichl, H.;*

Electronic Components and Technology Conference, 2001.

Proceedings., 51st , 29 May-1 June 2001

Page(s): 810 -815

[\[Abstract\]](#) [\[PDF Full-Text \(1608 KB\)\]](#) **IEEE CNF**

---

**11 Adoption of OPC and the impact on design and layout**

*Schellenberg, F.M.; Capodieci, L.; Socha, B.;*

Design Automation Conference, 2001. Proceedings , 18-22 June 2001

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[\[Abstract\]](#) [\[PDF Full-Text \(344 KB\)\]](#) **IEEE CNF**

---

**12 Testing the printability of VLSI layouts**

*Martins, R.; Kirchauer, H.;*

Integrated Circuits and Systems Design, 2001, 14th Symposium on. , 10-15 Sept. 2001

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[\[Abstract\]](#) [\[PDF Full-Text \(800 KB\)\]](#) **IEEE CNF**

---

**13 Evaluation of high transmittance attenuated phase shifting mask for 157 nm lithography**

*Yamabe, O.; Watanabe, K.; Itani, T.;*

Microprocesses and Nanotechnology Conference, 2001 International , 31 Oct.-2 Nov. 2001

Page(s): 312 -313

[\[Abstract\]](#) [\[PDF Full-Text \(300 KB\)\]](#) **IEEE CNF**

---

**14 Hierarchical fault diagnosis of analog integrated circuits**

*Chung Kin Ho; Shepherd, P.R.; Eberhardt, F.; Tenten, W.;*  
Circuits and Systems I: Fundamental Theory and Applications, IEEE  
Transactions on , Volume: 48 Issue: 8 , Aug. 2001  
Page(s): 921 -929

[\[Abstract\]](#) [\[PDF Full-Text \(144 KB\)\]](#) **IEEE JNL**

---

**15 High-throughput high-density mapping and spectrum  
analysis of transistor gate length variations in SRAM circuits**

*Xu Ouyang; Deeter, T.; Berglund, C.N.; Pease, R.F.W.; Lee, J.;*  
*McCord, M.A.;*  
Semiconductor Manufacturing, IEEE Transactions on , Volume: 14  
Issue: 4 , Nov. 2001  
Page(s): 318 -329

[\[Abstract\]](#) [\[PDF Full-Text \(362 KB\)\]](#) **IEEE JNL**

---

**16 Flip chip pad structure for high density organic build up  
substrate**

*Nakamura, K.; Harazono, M.; Yamashita, H.; Ding, D.H.; Baker, J.;*  
*Dubey, A.;*  
Electronics Packaging Technology Conference, 2000. (EPTC 2000).  
Proceedings of 3rd , 5-7 Dec 2000  
Page(s): 283 -285

[\[Abstract\]](#) [\[PDF Full-Text \(172 KB\)\]](#) **IEEE CNF**

---

**17 A new CMAC neural network architecture and its ASIC  
realization**

*Yuan-Pao Hsu; Kao-Shing Hwang; Chien-Yuan Pao; Jinn-Shyan*  
*Wang;*  
Design Automation Conference, 2000. Proceedings of the ASP-DAC  
2000. Asia and South Pacific , 25-28 Jan. 2000  
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[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) **IEEE CNF**

---

**18 A novel filtering method to extract three critical yield loss  
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*Imai, K.; Kaga, T.;*  
Semiconductor Manufacturing, IEEE Transactions on , Volume: 13  
Issue: 4 , Nov. 2000  
Page(s): 408 -415

[\[Abstract\]](#) [\[PDF Full-Text \(288 KB\)\]](#) **IEEE JNL**

---

**19 Intra-field gate CD variability and its impact on circuit performance**

*Orshansky, M.; Milor, L.; Ly Nguyen; Hill, G.; Yeng Peng; Chenming Hu;*

Electron Devices Meeting, 1999. IEDM Technical Digest. International , 5-8 Dec. 1999

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[\[Abstract\]](#) [\[PDF Full-Text \(456 KB\)\]](#) **IEEE CNF**

---

**20 A novel approach to simulate the effect of optical proximity on MOSFET parametric yield**

*Balasinski, A.; Gangala, H.; Axelrad, V.; Boksha, V.;*

Electron Devices Meeting, 1999. IEDM Technical Digest. International , 5-8 Dec. 1999

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[\[Abstract\]](#) [\[PDF Full-Text \(336 KB\)\]](#) **IEEE CNF**

---

**21 Highly accurate extraction of 3 critical yield loss components (gross, repeated, and random) by FIMER**

*Imai, K.; Kaga, T.;*

Semiconductor Manufacturing Conference Proceedings, 1999 IEEE International Symposium on , 11-13 Oct. 1999

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[\[Abstract\]](#) [\[PDF Full-Text \(420 KB\)\]](#) **IEEE CNF**

---

**22 Minimized power consumption for scan-based BIST**

*Gerstendorfer, S.; Wunderlich, H.-J.;*

Test Conference, 1999. Proceedings. International , 28-30 Sept. 1999

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[\[Abstract\]](#) [\[PDF Full-Text \(680 KB\)\]](#) **IEEE CNF**

---

**23 A new filtering method to extract repeated defects (FIMER) [lithography]**

*Imai, K.; Kaga, T.;*

Statistical Metrology, 1999. IWSM. 1999 4th International Workshop on , 12 June 1999

Page(s): 22 -25

[\[Abstract\]](#) [\[PDF Full-Text \(380 KB\)\]](#) [IEEE CNF](#)

---

**24 Control systems for the nanolithography process**

*Schaper, C.D.; El-Awady, K.; Tay, A.; Kailath, T.;*

Decision and Control, 1999. Proceedings of the 38th IEEE Conference on , Volume: 4 , 7-10 Dec. 1999

Page(s): 4173 -4178 vol.4

[\[Abstract\]](#) [\[PDF Full-Text \(564 KB\)\]](#) [IEEE CNF](#)

---

**25 Analysis of the impact of proximity correction algorithms on circuit performance**

*Li Chen; Milor, L.S.; Ouyang, C.H.; Maly, W.; Yeng-Kaung Peng;*

Semiconductor Manufacturing, IEEE Transactions on , Volume: 12 Issue: 3 , Aug. 1999

Page(s): 313 -322

[\[Abstract\]](#) [\[PDF Full-Text \(284 KB\)\]](#) [IEEE JNL](#)

---

**26 The K-model: RF IC modelling for communication systems simulation**

*Moult, L.; Chen, J.E.;*

Analog Signal Processing (Ref. No. 1998/472), IEE Colloquium on , 28 Oct. 1998

Page(s): 11/1 -11/8

[\[Abstract\]](#) [\[PDF Full-Text \(560 KB\)\]](#) [IEE CNF](#)

---

**27 A novel CMOS compatible multi-level flash EEPROM for embedded applications**

*Concannon, A.; McCarthy, D.; Mathewson, A.; Guillaumot, B.;*

*Papadas, C.; Kelaidis, C.;*

Device Research Conference Digest, 1998. 56th Annual , 22-24 June 1998

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[\[Abstract\]](#) [\[PDF Full-Text \(364 KB\)\]](#) [IEEE CNF](#)

---

**28 How faults can be simulated in self-testable VLSI digital circuits?**

*Bojanowicz, D.;*

Euromicro Conference, 1998. Proceedings. 24th , Volume: 1 , 25-27 Aug. 1998

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[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) **IEEE CNF**

---

**29 Gate oxide integrity testing on SOI wafers without test structure fabrication**

*Henaus, S.; Mondon, F.; Reimbold, G.; Moriceau, H.; Barge, T.; Auberton-Herve, A.J.;*

SOI Conference, 1998. Proceedings., 1998 IEEE International , 5-8 Oct. 1998

Page(s): 87 -88

[\[Abstract\]](#) [\[PDF Full-Text \(176 KB\)\]](#) **IEEE CNF**

---

**30 Testing technique for embedded ADC**

*Zagursky, V.; Gertners, A.;*

Circuits and Systems, 1998. IEEE APCCAS 1998. The 1998 IEEE Asia-Pacific Conference on , 24-27 Nov. 1998

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[\[Abstract\]](#) [\[PDF Full-Text \(308 KB\)\]](#) **IEEE CNF**

---

**31 Design and simulation tools for integrated optic circuits**

*Amersfoort, M.R.;*

Lasers and Electro-Optics Society Annual Meeting, 1998. LEOS '98. IEEE , Volume: 1 , 1-4 Dec. 1998

Page(s): 386 -387 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(184 KB\)\]](#) **IEEE CNF**

---

**32 Fault characterization of low capacitance full-swing BiCMOS logic circuits**

*Aziz, S.M.; Kamruzzaman, J.;*

Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian , 2-4 Dec. 1998

Page(s): 119 -123

[\[Abstract\]](#) [\[PDF Full-Text \(64 KB\)\]](#) **IEEE CNF**

---

**33 Highly scalable and fully logic compatible SRAM cell technology with metal damascene process and W local interconnect**

*Inohara, M.; Oyamatsu, H.; Unno, Y.; Fukaura, Y.; Goto, S.; Egi, Y.; Kinugawa, M.;*

VLSI Technology, 1998. Digest of Technical Papers. 1998 Symposium

on , 9-11 June 1998

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[\[Abstract\]](#) [\[PDF Full-Text \(296 KB\)\]](#) **IEEE CNF**

---

**34 Enhancement of underfill performance for flip-chip applications by use of silane additives**

*Vincent, M.B.; Meyers, L.; Wong, C.P.;*

Electronic Components and Technology Conference, 1998. 48th IEEE , 25-28 May 1998

Page(s): 125 -131

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---

**35 Automated extraction of capacitances and electrostatic forces in MEMS and ULSI interconnects from the mask layout**

*Bachtold, M.; Taschini, S.; Korvink, J.G.; Baltes, H.;*

Electron Devices Meeting, 1997. Technical Digest., International , 7-10 Dec. 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(844 KB\)\]](#) **IEEE CNF**

---

**36 Spice simulation of 0.18  $\mu\text{m}$  CMOS ring oscillators using physical models for capacitance and series resistance**

*Biesemans, S.; Kubicek, S.; De Meyer, K.;*

Electron Devices Meeting, 1997. Technical Digest., International , 7-10 Dec. 1997

Page(s): 141 -144

[\[Abstract\]](#) [\[PDF Full-Text \(260 KB\)\]](#) **IEEE CNF**

---

**37 Characterization techniques for mixed signal system**

*Zagursky, V.;*

AUTOTESTCON '97. 1997 IEEE Autotestcon Proceedings , 22-25 Sept. 1997

Page(s): 403 -407

[\[Abstract\]](#) [\[PDF Full-Text \(396 KB\)\]](#) **IEEE CNF**

---

**38 Optimization of  $f_T$ ,  $BV_{CEO}$  and  $\beta$ ; with selectively implanted collectors in BiCMOS technology**

*Guvench, M.G.;*

University/Government/Industry Microelectronics Symposium, 1997.,

Proceedings of the Twelfth Biennial , 20-23 July 1997

Page(s): 118 -122

[\[Abstract\]](#) [\[PDF Full-Text \(440 KB\)\]](#) **IEEE CNF**

---

**39 Generation and verification of tests for analogue circuits subject to process parameter deviations**

*Spinks, S.J.; Chalk, C.D.; Bell, I.M.; Zwolinski, M.;*

Defect and Fault Tolerance in VLSI Systems, 1997. Proceedings., 1997 IEEE International Symposium on , 20-22 Oct. 1997

Page(s): 100 -108

[\[Abstract\]](#) [\[PDF Full-Text \(460 KB\)\]](#) **IEEE CNF**

---

**40 A novel planarization technique for a high-T<sub>c</sub> multilevel IC process**

*Marathe, A.P.; Van Duzer, T.; Lee, L.P.;*

Applied Superconductivity, IEEE Transactions on , Volume: 7 Issue: 4 , Dec. 1997

Page(s): 3834 -3839

[\[Abstract\]](#) [\[PDF Full-Text \(288 KB\)\]](#) **IEEE JNL**

---

**41 Automated evaluation of critical features in VLSI layouts based on photolithographic simulations**

*Sengupta, C.; Cavallaro, J.R.; Wilson, W.L., Jr.; Tittel, F.K.;*

Semiconductor Manufacturing, IEEE Transactions on , Volume: 10 Issue: 4 , Nov. 1997

Page(s): 482 -494

[\[Abstract\]](#) [\[PDF Full-Text \(1040 KB\)\]](#) **IEEE JNL**

---

**42 Capacity planning for development wafer fab expansion**

*Chou, W.; Everton, J.;*

Advanced Semiconductor Manufacturing Conference and Workshop, 1996. ASMC 96 Proceedings. IEEE/SEMI 1996 , 12-14 Nov. 1996

Page(s): 17 -22

[\[Abstract\]](#) [\[PDF Full-Text \(488 KB\)\]](#) **IEEE CNF**

---

**43 Laminated high-aspect-ratio microstructures in a conventional CMOS process**

*Fedder, G.K.; Santhanam, S.; Reed, M.L.; Eagle, S.C.; Guillou, D.F.; Lu, M.S.-C.; Carley, L.R.;*

Micro Electro Mechanical Systems, 1996, MEMS '96, Proceedings. 'An

Investigation of Micro Structures, Sensors, Actuators, Machines and Systems'. IEEE, The Ninth Annual International Workshop on , 11-15 Feb. 1996  
Page(s): 13 -18

[\[Abstract\]](#) [\[PDF Full-Text \(1188 KB\)\]](#) **IEEE CNF**

---

**44 A study involving the design and the fabrication process on the SRAM behaviour during a dose-rate event**

*Marec, R.; Mary, P.; Gaillard, R.; Palau, J.-M.; Bruguier, G.; Gasiot, J.;*

Nuclear Science, IEEE Transactions on , Volume: 43 Issue: 3 , June 1996

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[\[Abstract\]](#) [\[PDF Full-Text \(612 KB\)\]](#) **IEEE JNL**

---

**45 Extracting solid conductors from a single triangulated surface representation for interconnect analysis**

*Sefler, J.F.; Neureuther, A.R.;*

Semiconductor Manufacturing, IEEE Transactions on , Volume: 9 Issue: 1 , Feb. 1996

Page(s): 82 -86

[\[Abstract\]](#) [\[PDF Full-Text \(656 KB\)\]](#) **IEEE JNL**

---

**46 Layout-based 3D solid modeling for IC**

*Zhiping Yu; Wang, K.; Tao Chen; Dutton, R.W.; Watt, J.T.;*

VLSI Technology, Systems, and Applications, 1995. Proceedings of Technical Papers., 1995 International Symposium on , 31 May-2 June 1995

Page(s): 108 -112

[\[Abstract\]](#) [\[PDF Full-Text \(412 KB\)\]](#) **IEEE CNF**

---

**47 Simulating IC reliability with emphasis on process-flaw related early failures**

*Moosa, M.S.; Poole, K.F.;*

Reliability, IEEE Transactions on , Volume: 44 Issue: 4 , Dec. 1995

Page(s): 556 -561

[\[Abstract\]](#) [\[PDF Full-Text \(620 KB\)\]](#) **IEEE JNL**

---

**48 Fabrication of vapor-deposited micro heat pipe arrays as an integral part of semiconductor devices**

*Mallik, A.K.; Peterson, G.P.; Weichold, M.H.;*  
Microelectromechanical Systems, Journal of , Volume: 4 Issue: 3 ,  
Sept. 1995  
Page(s): 119 -131

[\[Abstract\]](#) [\[PDF Full-Text \(1012 KB\)\]](#) **IEEE JNL**

---

49 **A design system for on-chip oversampling A/D interfaces**

*Mar, M.F.; Brodersen, R.W.;*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on ,  
Volume: 3 Issue: 3 , Sept. 1995

Page(s): 345 -354

[\[Abstract\]](#) [\[PDF Full-Text \(1056 KB\)\]](#) **IEEE JNL**

---

50 **Simulation and experimental study of gray-tone**

**lithography for the fabrication of arbitrarily shaped surfaces**

*Henke, W.; Hoppe, W.; Quenzer, H.J.; Staudt-Fischbach, P.; Wagner, B.;*

Micro Electro Mechanical Systems, 1994, MEMS '94, Proceedings,  
IEEE Workshop on , 25-28 Jan. 1994

Page(s): 205 -210

[\[Abstract\]](#) [\[PDF Full-Text \(1224 KB\)\]](#) **IEEE CNF**

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Harvey, M.C.; Lott, J.A.; Nelson, T.R., Jr.; Stintz, A.; Malloy, K.J.;  
Semiconductor Laser Conference, 2002. IEEE 18th International , 29  
Sept.-3 Oct. 2002  
Page(s): 11 -12

[\[Abstract\]](#) [\[PDF Full-Text \(249 KB\)\]](#) **IEEE CNF****2 Engineering of effective quadratic and cubic nonlinearities in two-period QPM gratings**

Bang, O.; Clausen, C.B.; Torner, L.;  
Lasers and Electro-Optics, 2000. (CLEO 2000). Conference on , 7-12  
May 2000  
Page(s): 147 -148

[\[Abstract\]](#) [\[PDF Full-Text \(160 KB\)\]](#) **IEEE CNF****3 High Q metal strip SSBW resonators using a SAW design**

Avramov, I.D.;  
Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions  
on , Volume: 37 Issue: 6 , Nov. 1990  
Page(s): 530 -534

[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) **IEEE JNL****4 Imaging Polarimeter Arrays for Near-Millimeter Waves**

Tong, P.P.; Neikirk, D.P.; Young, P.E.; Peebles, W.A., Jr.; Luhmann,  
M.C., Jr.;  
Antennas and Propagation Society International Symposium, 1999. IEEE  
AP-S 99 , Volume: 1 Issue: 1 , 1999  
Page(s): 100 -103

*N.C.; Rutledge, D.B.;*

Microwave Theory and Techniques, IEEE Transactions on , Volume:  
32 Issue: 5 , May 1984

Page(s): 507 -512

[\[Abstract\]](#) [\[PDF Full-Text \(1000 KB\)\]](#) **IEEE JNL**

---

**5 Laser coding of bipolar read-only memories**

*North, J.C.; Weick, W.W.;*

Solid-State Circuits, IEEE Journal of , Volume: 11 Issue: 4 , Aug 1976

Page(s): 500 -505

[\[Abstract\]](#) [\[PDF Full-Text \(1008 KB\)\]](#) **IEEE JNL**

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 D. W. Hightower , B. A. Unger**Proceedings of the ninth design automation workshop on Design automation** June 1972

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Chad D. DeJong , Seth A. Fischbein

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